CLAIMS

1. A method for packaging a microelectronic substrate, comprising:

disposing an encapsulating material adjacent to a surface of the microelectronic substrate; and

exposing at least a portion of the surface of the microelectronic substrate by removing a portion of the encapsulating material adjacent to the surface of the microelectronic substrate with the microelectronic substrate in an operable condition after the portion of the encapsulating material is removed.

2. The method of claim 1 wherein the microelectronic substrate has a first surface and a second surface facing opposite the first surface, the first surface having a plurality of bond sites for electrical connections to the microelectronic substrate, and further wherein exposing a portion of a surface of the microelectronic substrate includes exposing a portion of the second surface of the microelectronic substrate.

3. The method of claim 1, further comprising:

mounting the microelectronic substrate to a support member with a first surface of the microelectronic substrate facing the support member and a second surface of the microelectronic substrate facing away from the support member;

electrically coupling the microelectronic substrate to the support member;

disposing the encapsulating material adjacent to both the microelectronic substrate and the support member; and

exposing at least a portion of the second surface of the microelectronic substrate by directing laser radiation toward the portion of the encapsulating material adjacent to the second surface to ablate the portion of the encapsulating material.

4. The method of claim 1, further comprising:

selecting the microelectronic substrate to include a memory chip;

mounting the microelectronic substrate to a printed circuit board; and

disposing the encapsulating material adjacent to both the printed circuit board and the microelectronic substrate.

5. The method of claim 1, further comprising transferring heat directly away from the exposed portion of the surface of the microelectronic substrate.

6. The method of claim 1, further comprising convectively transferring heat directly away from the exposed portion of the surface of the microelectronic substrate.

7. The method of claim 1 wherein removing a portion of the encapsulating material includes directing laser radiation toward the encapsulating material.

8. The method of claim 1 wherein removing the portion of the encapsulating material includes directing a laser beam having a power of from about 4 watts to about 25 watts toward the encapsulating material.

9. The method of claim 1 wherein removing the portion of the encapsulating material includes sequentially removing layers of the portion of the encapsulating material by sequentially exposing the layers of encapsulating material to laser radiation.

Sub A3

10. A method for packaging a microelectronic substrate, comprising:

disposing an encapsulating material adjacent to the microelectronic substrate; and

forming a heat transfer structure in an external surface of the encapsulating material by manipulating at least a portion of the encapsulating material to define at least one exposed heat transfer surface of the heat transfer structure.

11. The method of claim 10 wherein manipulating at least a portion of the encapsulating material includes removing a portion of encapsulating material by directing laser radiation toward the encapsulating material.

12. The method of claim 10 wherein the microelectronic substrate has a first surface and a second surface facing opposite the first surface, the first surface having a plurality of bond sites for electrical connections to the microelectronic substrate, and further wherein manipulating at least a portion of the encapsulating material includes removing a portion of the encapsulating material adjacent to the second surface of the microelectronic substrate.

13. The method of claim 10, further comprising:

mounting the microelectronic substrate to a support member;

electrically coupling the microelectronic substrate to the support member;

disposing the encapsulating material adjacent to both the microelectronic substrate and the support member; and

removing at least a portion of the encapsulating material from a region proximate to the microelectronic substrate.

14. The method of claim 10 wherein manipulating the encapsulating material includes removing a portion of the encapsulating material to expose a portion of a surface of the microelectronic substrate initially covered by the encapsulating material.

15. The method of claim 10 wherein forming a heat transfer structure includes forming a cylindrical rod of encapsulating material projecting away from the microelectronic substrate.

16. The method of claim 10 wherein forming a heat transfer structure includes forming a rib projecting away from the microelectronic substrate.

17. A method for packaging a microelectronic substrate, comprising:

positioning at least one of an encapsulating material and a support member adjacent to the microelectronic substrate; and

processing at least one of the encapsulating material and the support member to have an interlocking feature by manipulating a portion of the encapsulating material and/or

the support member, the interlocking feature being configured to engage with a corresponding interlocking feature of another microelectronic substrate.

18. The method of claim 17 wherein manipulating a portion of the encapsulating material and/or the support member includes directing laser radiation toward the encapsulating material and/or the support member to ablate the portion of the encapsulating material and/or the support member.

19. The method of claim 17 wherein the interlocking feature is positioned in a first surface of the encapsulating material and wherein the method further comprises forming a second interlocking feature in a second surface of the encapsulating material facing opposite the first surface.

20. The method of claim 17 wherein processing the encapsulating material includes forming a recess in the encapsulating material.

21. The method of claim 17 wherein processing the encapsulating material includes forming a projection in the encapsulating material extending away from the microelectronic substrate.

22. The method of claim 17 wherein the microelectronic substrate is electrically coupled to the support member and the interconnecting feature is a first feature formed in the encapsulating material, and wherein the method further comprises processing the support member to form a second interconnecting feature configured to engage the first interconnecting feature of another microelectronic substrate.

23. A method for positioning microelectronic device packages, comprising:

aligning a first microelectronic device package having a first microelectronic substrate and a first encapsulant with a second microelectronic device package having a second microelectronic substrate and a second encapsulant; and

engaging a first interlocking feature of the first microelectronic device package with a second interlocking feature of the second microelectronic device package to at least restrict relative motion between the first and second microelectronic device packages.

24. The method of claim 23, further comprising engaging a tab of the first encapsulant of the first microelectronic device package with a recess in the second encapsulant of the second microelectronic device package.

25. The method of claim 23 wherein the first microelectronic device package includes a support member having a cavity, and wherein the method further comprises receiving the second encapsulant of the second microelectronic device package in the cavity of the support member of the first microelectronic device package.

26. A method for packaging a microelectronic substrate, comprising:

electrically coupling the microelectronic substrate to a support member having a first surface and a second surface facing opposite the first surface, the first surface having a conductive bond pad;

positioning the support member and the microelectronic substrate between two portions of a mold with the first surface and the bond pad of the support member facing a first cavity in the first portion of the mold and the microelectronic substrate facing a second cavity in the second portion of the mold;

disposing an encapsulating material in the first and second cavities of the mold to engage the microelectronic substrate and the bond pad; and

removing a portion of the encapsulating material covering the bond pad to expose the bond pad while the microelectronic substrate remains in an operable condition.

27. The method of claim 26, further comprising:

aligning a first edge of the first cavity with a second edge of the second cavity; and

rigidly supporting the support member in the mold by clamping the support member between the first and second edges.

28. The method of claim 26 wherein removing the portion of the encapsulating material includes directing laser radiation toward the encapsulating material and ablating the portion of the encapsulating material.

29. The method of claim 26 wherein removing the portion of the encapsulating material includes directing a laser beam having a power of from about 4 watts to about 25 watts toward the encapsulating material.

30. The method of claim 26 wherein removing the portion of the encapsulating material includes sequentially removing layers of the portion of the encapsulating material by sequentially exposing the encapsulating material to laser radiation.

31. The method of claim 26, further comprising attaching a solder ball to the bond pad.

32. A method for packaging a microelectronic substrate, comprising:

mounting the microelectronic substrate to a support member with a first surface of the microelectronic substrate facing the support member and a second surface of the microelectronic substrate facing opposite the first surface;

electrically coupling the microelectronic substrate to the support member by passing wire bonds though an aperture in the support member and connecting one end of each wire bond to the support member and an opposite end of each wire bond to the microelectronic substrate;

encapsulating the microelectronic substrate and the support member by disposing an encapsulating material over the support member and the second surface of the microelectronic substrate; and

directing a source of laser radiation toward the second surface of the microelectronic substrate to remove at least a portion of the encapsulating material adjacent to the second surface and expose the second surface.

33. The method of claim 32, further comprising forming a heat transfer feature in the encapsulating material by removing a portion of the encapsulating material to define an exposed external surface of the heat transfer feature.

34. The method of claim 32 wherein directing the source of laser radiation includes directing a laser beam having a power of from about 4 watts to about 25 watts.

35. The method of claim 32 wherein directing the source of laser radiation includes engaging a laser beam with the encapsulating material to remove a first portion of the encapsulating material and engaging the laser beam with the encapsulating material again to remove a second portion of the encapsulating material initially covered by the first portion of the encapsulating material.

36. The method of claim 32 wherein removing a portion of the encapsulating material includes removing a layer of encapsulating material having a thickness of greater than about 0.003 inch.

37. A microelectronic device package formed by a process, comprising:

disposing an encapsulating material adjacent to the microelectronic substrate; and

exposing at least a portion of a surface of the microelectronic substrate by removing a portion of the encapsulating material adjacent to the surface of the microelectronic substrate with the microelectronic substrate in an operable condition after the portion of the encapsulating material is removed.

38. The device package of claim 37 wherein the microelectronic substrate has a first surface and a second surface facing opposite the first surface, the first surface having a plurality of bond sites for electrical connections to the microelectronic substrate, and further wherein exposing a portion of a surface of the microelectronic substrate includes exposing a portion of the second surface of the microelectronic substrate.

39. The device package of claim 37, further comprising removing a portion of the encapsulating material by directing laser radiation toward the portion of the encapasulating material to ablate the portion of the encapsulating material.

40. A microelectronic device package, comprising:

an operable microelectronic die having at least one integrated circuit and a die surface; and

an encapsulating material covering at least a portion of the microelectronic die, the encapsulating material having an external surface and an aperture extending through the external surface to the die surface with a portion of the die surface exposed through the aperture.

41. The package of claim 40, further comprising a support member adjacent to the microelectronic die, and further wherein the microelectronic die is electrically coupled to the support member.

42. The package of claim 40 wherein the microelectronic die has a first surface and a second surface facing opposite the first surface, the first surface having a plurality of terminals for electrical connections to the microelectronic die, the second surface being exposed through the aperture in the encapsulating material.

43. The package of claim 40 wherein the encapsulating material includes heat transfer structures extending transverse to the die surface, the heat transfer structures having exposed, spaced-apart external heat transfer surfaces.

44. The package of claim 40 wherein the encapsulating material includes an interlocking feature positioned to engage a corresponding interlocking feature of another device package to at least resist relative movement between the device packages.

45. A microelectronic device package, comprising:

an operable microelectronic substrate having a first surface and a second surface facing opposite the first surface; and

an encapsulating material and/or a support member covering at least a portion of at least one of the first and second surfaces of the microelectronic substrate, the encapsulating material and/or the support member having an interlocking feature positioned to engage a corresponding interlocking feature of another device package and at least restrict relative movement between the device packages when the interlocking features of the packages are engaged with each other.

46. The device package of claim 45 wherein the microelectronic substrate is at least partially encased in an encapsulating material and the interlocking feature includes a projection in the encapsulating material extending away from the second surface of the microelectronic substrate and positioned to be received in a corresponding recess of the other device package.

47. The device package of claim 45 wherein the interlocking feature includes a recess in the encapsulating material positioned to receive a projection of the other device package.

48. The device package of claim 45, wherein the microelectronic substrate is attached to a support member and the interlocking feature includes a recess in the support member.

49. A pair of microelectronic device packages, comprising:

a first microelectronic device package having a first microelectronic substrate and a first encapsulating material at least partially covering the first microelectronic substrate, the first encapsulating material having an external surface and an aperture in the external surface; and

a second microelectronic device package having a second microelectronic substrate and a second encapsulating material at least partially covering the second

microelectronic substrate, the second encapsulating material having an external surface and a projection extending away from the external surface, the projection being aligned with and received in the aperture of the first encapsulating material when the first microelectronic substrate is adjacent to the second microelectronic substrate.

50. The device packages of claim 49, further comprising a first support member electrically coupled to the first microelectronic substrate and a second support member electrically coupled to the second microelectronic substrate.

51. The device packages of claim 49 wherein at least one of the encapsulating materials includes a heat transfer structure extending transverse to the substrate surface, the heat transfer structures having exposed, spaced-apart external heat transfer surfaces.

52. A microelectronic device package, comprising:

a support member having a conductive link with a first terminal and a second terminal, the second terminal having a bonding surface to form electrical connections with the second terminal;

a microelectronic substrate engaged with the support member and electrically coupled to the first terminal of the conductive link; and

an encapsulating material at least partially covering the microelectronic substrate and the support member, the encapsulating material extending over at least a substantial portion of the bonding surface of the second terminal of the conductive link.

53. The package of claim 52 wherein the support member includes a printed circuit board, the first terminal of the conductive link includes a wire bond pad coupled with a wire bond to the microelectronic substrate, and the second terminal includes a solder ball pad.

54. The package of claim 52 wherein the support member includes a printed circuit board having an aperture, and wherein the package further comprises a wire bond extending through the aperture from the microelectronic substrate to the first terminal.

55. The package of claim 52 wherein the encapsulating material includes an epoxy.

56. A microelectronic device package, comprising:

a microelectronic substrate having a substrate surface; and

an encapsulating material at least partially covering the microelectronic substrate, the encapsulating material defining a plurality of heat transfer structures projecting away from the substrate surface, each heat transfer structure having at least one exposed, external heat transfer surface spaced apart from and facing a heat transfer surface of another of the heat transfer structures.

57. The package of claim 56 wherein the encapsulating material includes an epoxy.

58. The package of claim 56 wherein the heat transfer structures include at least one cylindrical rod of encapsulating material projecting away from the microelectronic substrate.

59. The package of claim 56 wherein the heat transfer structures include at least one rib projecting away from the microelectronic substrate.

60. The package of claim 56 wherein the encapsulating material has an aperture and the surface of the microelectronic substrate is exposed through the aperture in the encapsulating material.

61. A microelectronic device package, comprising:

a microelectronic substrate having a first surface and a second surface facing opposite the first surface;

a support member having a first surface engaged with the first surface of the microelectronic substrate and a second surface facing opposite the first surface, the support

member having an aperture extending therethrough from the first surface to the second surface;

a plurality of bond members extending through the aperture of the support member, the bond members being connected to the microelectronic substrate and the support member; and

an encapsulating material disposed adjacent to the microelectronic substrate and the support member, the encapsulating material having an opening through which a substantial portion of the second surface of the microelectronic substrate is exposed.

62. The package of claim 61 wherein the encapsulating material has at least one heat transfer structure proximate to the second surface of the microelectronic substrate, the heat transfer structure having an exposed external surface positioned to transfer heat from the microelectronic substrate.

63. The package of claim 61 wherein the encapsulating material includes an interlocking feature positioned to engage a corresponding interlocking feature of another package to at least resist relative movement between the packages.